CLAIMS

1. An exponent computation apparatus for performing either an overflow or underflow comparison while minimizing overflow/underflow comparison circuitry, said apparatus comprising:

overflow/underflow possible check circuitry, said overflow/underflow possible check circuitry configured to determine if a mathematical operation involving a first exponent signal and a second exponent signal creates a potential overflow condition, said overflow/underflow possible check circuitry configured to generate a signal indicating if said overflow condition is a possibility; and

exponent compare circuitry, said exponent compare circuitry configured to compute an actual overflow/underflow condition, said exponent compare circuitry configured to compute an actual overflow condition if said signal indicates overflow is possible, and said exponent compare circuitry configured to computes an actual underflow condition if said signal does not indicate overflow is possible.

2. The apparatus of claim 1, wherein said exponent compare circuitry generates an error signal if an actual overflow/underflow condition exists.

3. The apparatus of claim 2, further comprising:

pre-normalized exponent selection circuitry configured to determine a larger exponent between said first exponent signal and said second exponent signal.

4. The apparatus of claim 3, wherein said overflow/underflow possible check circuitry uses said largest exponent to determine if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

5. The apparatus of claim 3, further comprising:

exponent shift amount circuitry configured to determine how much the mantissa of said largest exponent must be shifted to be normalized, and configured to compute a normalized exponent.

6. The apparatus of claim 5, wherein said exponent compare circuitry uses said normalized exponent to determine if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

7. A method for performing an overflow and underflow comparison while minimizing overflow/underflow comparison circuitry, comprising the steps of:

receiving a first exponent signal and a second exponent signal;

determining if a mathematical operation involving said first exponent signal and said second exponent signal creates a potential overflow condition;

generating a signal indicating if said potential overflow condition exists;

computing an actual overflow condition if said signal indicates said potential overflow condition exists; and

computing an actual underflow condition if said signal indicates said potential overflow condition does not exist.

8. The method of claim 7, further comprising the steps of:

generating an overflow error signal if an actual overflow condition exist; and

generating an underflow error signal if an actual underflow condition exist.

9. The method of claim 7, further comprising the step of:

determining a largest exponent between said first exponent signal and said second exponent signal.

10. The method of claim 9, further comprising the step of:

using said largest exponent to determine if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

11. The method of claim 9, further comprising the steps of:

determining how much a mantissa of said largest exponent must be shifted to be normalized, and

computing a normalized exponent.

12. The method of claim 11, further comprising the steps of:

using said normalized exponent to determines if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

13. An exponent computation apparatus for performing an overflow and underflow comparison while minimizing overflow/underflow comparison circuitry, the apparatus comprising:

means for receiving a first exponent signal and a second exponent signal;

means for determining if a mathematical operation involving said first exponent signal and said second exponent signal creates a potential overflow condition;

means for generating a signal indicating if said potential overflow condition exists; and

means for computing, wherein said computing means computes an actual overflow condition if said signal indicates said potential overflow condition exists, and wherein said computing means computes an actual underflow condition if said signal indicates said potential overflow condition does not exist.

14. The apparatus of claim 13, wherein said computing means further comprises:

means for generating an overflow error signal if an actual overflow condition exist; and

means for generating an underflow error signal if an actual underflow condition exist..

15. The apparatus of claim 13, further comprising:

means for determining a largest exponent between said first exponent signal and said second exponent signal.

16. The apparatus of claim 13, wherein said computing means further comprises:

means for using said largest exponent to determine if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

17. The apparatus of claim 14, further comprising:

means for determining how much a mantissa of said largest exponent must be shifted to be normalized, and

means for computing a normalized exponent.

18. The apparatus of claim 17, wherein said computing means further comprises:

means for using said normalized exponent to determines if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

19. An exponent compare apparatus for computing either an overflow or underflow condition, the apparatus comprising:

a plurality of constant selectors, wherein each of said plurality of constant selectors selects an exponent precision underflow/overflow constant from a plurality of exponent underflow/overflow constants;

a plurality of carry save adders, wherein each of said plurality of carry save adders generate a sum signal and carry signal from one of said plurality of exponent precision underflow/overflow constants, a pre-normalized exponent signal and a normalization shift amount signal;

at plurality of comparators, wherein each of said comparators computes an underflow/overflow result from said sum signal and said carry signal; and

at plurality of underflow/overflow result selector, wherein each of said underflow/overflow result selector indicates an underflow/overflow condition from said underflow/overflow result and an exponent adjust amount signal.

20. The apparatus of claim 19, wherein said plurality of constant selectors further comprises two constant selectors.

21. The apparatus of claim 19, wherein said plurality of carry save adders further comprises two carry save adders.

22. The apparatus of claim 19, wherein said plurality of comparators further comprises four comparators and wherein a first one of said four comparators uses a least significant bit input of said carry signal from one of said plurality of carry save adders and a carry-in signal to extend the range of said constants being compared.

23. An exponent compare apparatus for computing either an overflow or underflow condition, the apparatus comprising:

means for selecting an exponent precision underflow/overflow constant from a plurality of exponent underflow/overflow constants;

means for generating a sum signal and carry signal from one of said plurality of exponent precision underflow/overflow constants, a pre-normalized exponent signal and a normalization shift amount signal;

means for computing an underflow/overflow result from said sum signal and said carry signal; and

means for selecting an underflow/overflow result that indicates an underflow/overflow condition from said underflow/overflow result and an exponent adjust amount signal.

24. The apparatus of claim 23, wherein said means for selecting further comprises two constant selectors.

25. The apparatus of claim 23, wherein said generating means further comprises two carry save adders.

26. The apparatus of claim 23, wherein said computing means further comprises four comparators, wherein a first one of said four comparators uses a least significant bit input of said carry signal from one of said plurality of carry save adders and a carry-in signal to extend the range of said constants being compared.